Recent Advances in GaN Power HEMTs Related to Thermal Problems and Low-Cost Approaches

WW05
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Thermal management of electronics: Measurement and the limits of GaN-on-diamond electronics

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Outline

- GaN electronics
- Thermal management challenges
- Thermal materials and device characterization
- Ultra-high power electronics: GaN-on-Diamond HEMTs
- Conclusions
Microwave GaN Electronics

You can buy this already (GaN-on-SiC, GaN-on-Si) !!!

Thermal management

Challenges: New material and device design; how to measure channel temperature of a device?
Performance and reliability

Device degradation is temperature and electric field accelerated.

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Electric field & temperature

Electric fields can be ‘shaped’ using e.g. field plates, T-shaped gate, slanted gate i.e., electric field driven device degradation can be limited.

Temperature is the main factor at present limiting the reliability i.e. determining the maximum possible power density.
GaN HEMT thermal history

**Worked example 20W 10GHz solid-state module**

- **GaAs pHEMT**
  - $V_{ds}=8V$ (0.9W/mm)
  - 4 x 1.38mm transistor
  - $Z_{opt}=4.5\,\text{ohm} // 1.1\,\text{pF}$

- **GaN HEMT**
  - $V_{ds}=28V$ (5W/mm)
  - 1 x 1mm transistor
  - $Z_{opt}=50\,\text{ohm} // 0.2\,\text{pF}$

**GaAs (0.5 W/mK) thermal conductivity much lower than GaN-on-SiC (1.6; 4.5 W/mK).**

**Cell size determined by operating frequency**
- 4.47W
- 0.5dB manifold loss

**Presently**
- 4x reduction in size

**Is this the limit?**

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**Channel temperature**

Device degradation determined buy temperature

Rate of device failure $\propto \exp(-E_a/k_BT)$, with $E_a = \text{activation energy}$

$T = \text{channel temperature (or temperature at specific location inside channel)}.$

**Gate metal diffusion**

- Au
- Pt
- Ti

**J. A. del Alamo et al., IEEE IEDM 2004**
Why waste with experiment

1. Heater width?
2. I can do a thermal simulation ... this saves me a lot of money and time
3. Heat has to traverse interfaces

Thermal conductivity of material and variation through layer(s)

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IR Thermography

**Basic principle:** Measures intensity of thermal IR radiation

\[ u(\nu, T) = \frac{8\pi h\nu^3}{c^3} \exp \left( \frac{\hbar \nu}{k_B T} \right) - 1 \]

**Measured intensity** \( j = \sigma T^4 \)

with \( \sigma \) Stefan-Boltzmann constant

**Often** 3-5 \( \mu m \) or 8-10 \( \mu m \) spectral window is used.

**Fast, but** diffraction-limited spatial resolution of >3-10 \( \mu m \).
**IR Thermography**

**Limited lateral resolution:**

Typical ‘no’ depth resolution (for uncoated devices):

**IR:** 3-10 μm

often 2-5 μm

IR measures a temperature average which is often not easy to define.

**Electrical Methods**

**Basic principle:** Quantifies changes in IV curve with temperature rise, e.g., a change in saturation current.

**Advantage:** Uses electrical test equipment standard in most laboratories; measures however average temperature over whole device.
Raman thermography

Based on that vibrations of ‘atoms’ (phonons) of materials are temperature dependent

- Spatial resolution ~ 0.5-0.7 µm.
- Temperature resolution < 2-5 °C.
- Time resolution ~ 10 ns.
- Easy to use.

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The Raman method

Photons of a laser ‘hit’ device

- Light of same photon energy as laser
- Light of increased photon energy (photon absorbs a vibration of ‘atoms’)
- Light of reduced photon energy (photon created a vibration of ‘atoms’)

Scattered light contains three different wavelengths

A typical Raman spectrum

Temperature in ‘all’ different material layers in a device can be probed simultaneously:
- GaN, SiC temperature in GaN/SiC HEMT,
- AlGaAs, GaAs temperature in GaAs pHEMT,
- ...

Raman vs IR thermography

Spatial resolution: Raman $\approx 0.5-0.7$ μm  IR $\approx 7$ μm.
Importance of interfaces


How to obtain time resolution

Order of magnitude faster and more accurate than other thermography techniques.

Time-resolved Raman

Ability to trace temperature with 10ns time resolution


Can one improve resolution?

Solid Immersion Lens (SIL)

DC vs RF temperatures

Activation energy determined in DC and RF lifetime test similar.


However, for >100V

J.W. Pomeroy et al. ROCS 2015.
How to do it in real life?

Can be performed on-wafer or in-package. Only condition is that the semiconductor of the device is optically visible.

Temperature measured

For optically transparant materials – Average of temperature in small volume

For optically non-transparant materials – Small ‘surface’ area

Temperature average over 0.75 \( \mu m \times 0.75 \mu m \times 50nm \) (for GaAs)

It is well defined over which area an average of temperature is measured and should be compared a subsequent thermal simulation !!!
Simulation to aid experiment

If there is a T-gate or field plate, we consider this by using thermal simulation, as those ‘screen’ the hot spot.

Methodology developed ...

Step 1 – We fit in thermal simulation the gradient in temperature through SiC to extract SiC thermal conductivity.

Step 2 – We fit in thermal simulation any resistances at internal chip interfaces.

Step 3 – We measure temperature in active device region and determine Edge of Chip (EoC) temperature (temperature 500 μm away from device).

Step 4 – We fit thermal simulation to HEMT and EoC temperature; EoC temperature considers die attach.

Extract key material parameters
Thermal simulation

2D drift-diffusion model

3D finite element thermal model

Joule heating map

Calibrated 3D thermal model including die and package

This approach combines the advantage of accurate $P_{diss}$ profile (drift-diffusion) with 3D finite element, e.g. large models


Good repeatability

≤ ±5°C
GaN-on-Diamond HEMT

A 3x power density increase was achieved by the DARPA NJTT program.

Thermal conductivities

Single crystalline diamond

Enriched Diamond

Natural diamond

SiC thermal conductivity: 4.8 W/cmK

Single-crystalline diamond

Not a realistic option to use for semiconductor technology

Poly-crystalline diamond

Grain size

Defects

phonon-phonon
The role of interfaces

The Interface(s) of GaN on Diamond

GaN

SiN

Diamond

Polycrystalline diamond properties as well as interfaces need to be optimized.

Importance of interfaces
Fit finite element model by adjusting two parameters: $\text{Diamond thermal conductivity} + \text{GaN/diamond interface } TBR_{\text{eff}}$

$Pomeroy \text{ et al, } \text{CSICS 2014.}$

**Diamond thermal properties**

$TBR_{\text{eff}}$: Effective thermal boundary resistance

Effective thermal conductivity: Weighted average, influenced by grain size.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>T.C. [W/mK]</th>
<th>$TBR_{\text{eff}} \times 10^{-8}$ [m²K/W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN-on-SiC</td>
<td>420</td>
<td>2-5 (~2.5 typical)</td>
</tr>
<tr>
<td>GaN-on-di</td>
<td>1200 (effective)</td>
<td>2.7±0.3</td>
</tr>
</tbody>
</table>

 REMINDER: Bulk diamond: 2000-3000 W/mK

$Pomeroy \text{ et al, CSICS 2013}$
Near nucleation diamond

Grain evolution can be controlled by manipulating the chemistry of the diamond growth.

Diamond beyond nucleation

Thermal conductivity determined by 3-omega technique.
Modeling of diamond properties

(i) thermal resistance between grains,
(ii) shortening in the phonon mean free path due to the reduced size of the grains

\[
k^{KC}(T, \Gamma, L_{eff}, G) = \frac{k^C(T, \Gamma, L_{eff})}{1 + \frac{k^C(T, \Gamma, L_{eff})}{L_{eff} \times G}}
\]

Grain Boundary thickness


GaN-diamond interface
Transient Thermoreflectance

Varied thickness 28 nm to 100 nm

Presently we develop this into a commercial equipment.


Validation of the technique

Precautions have been taken to ensure that the measured signal represents the surface temperature transient.
- Different UV powers result in identical transients.
- Thermo-optic simulation further supports data.

H. Sun et al, CSManTech 2015
Dielectric seeding layer needs to be optimized.

- When substrate thermal conductivity is low, TBR\(_{\text{eff}}\) is not the major factor.
- However, TBR\(_{\text{eff}}\) limits heat removal for high thermal conductivity substrates.

H. Sun et al, CSMantech 2015
Wafer screening

Fast wafer-mapping of the GaN-on-Diamond thermal resistance

Materials:

- Two metallization levels:
  1. Drain contact
  2. Source field plate
- GaN

S Martin Horcajo et al., CS Mantech 2016
GaN-diamond HEMT design

Decreasing thermal resistance associated with the carrier enables a further Increase in power density to ~3X

GaN layer optimization

A 1µm-thick GaN buffer is optimal for the range TBR\textsubscript{eff} values expected
Raman experimental validation

We validate all thermal simulations with Raman thermography measurements.

GaN-diamond stability
Coefficient of thermal expansion

---

Stress in GaN layer

**Determined using Raman spectroscopy**

<table>
<thead>
<tr>
<th>Year</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>With nitride transition layers</strong></td>
<td>Tentative</td>
<td>Tentative</td>
<td>Tentative</td>
</tr>
<tr>
<td><strong>Without nitride transition layers</strong></td>
<td>Tentative</td>
<td>Tentative</td>
<td>Tentative</td>
</tr>
</tbody>
</table>

**Wafer**

Sun et al, CS Mantech 2016
How to test for stability?

High mechanical stability

We try to cause fracture at the GaN-diamond interface

**Estimation of interface strength**

GaN layer fractures as >3 GPa; GaN/diamond interface fracture strength is much greater.

**Thermomechanical stability**

Good thermo-mechanical stability in the areas studied is no change in the TBR after annealing.
Conclusions

- GaN electronics **main challenge** at present is its **heat sinking**.
- Raman thermography offers the opportunity to **quantify channel temperature**, and to identify and optimize thermal bottlenecks such as interfaces.
- Raman thermography enables **0.5µm spatial and 10ns time resolution** thermal imaging in 3D, which can be improved further using **solid immersion lenses (SILs)**.
- GaN-on-Diamond HEMTs enable **3x improvement in power density**, however, require optimization in diamond thermal properties near the interface and of the interface itself.
- **Transient thermoreflectance** can be used for wafer mapping of thermal interfaces (before device fabrication) and for device thermal analysis.
- **High mechanical & thermo-mechanical stability** of GaN-diamond interface was demonstrated.

Acknowledgment

**Research Professor & Research Fellows**
- Prof. Michael J. Uren
- Dr. James W. Pomeroy
- Dr. Dong Liu

**Postdoctoral Researchers**
- Dr. Julian Anaya
- Dr. Roland Baranyai
- Dr. Tommaso Brazzini
- Dr. Indranil Chatterjee
- Dr. Sara Horcajo
- Dr. Huarui Sun
- Dr. Serge Karbojan

**PhD students:**
- Peter Butler
- Callum Middleton
- Bahar Oner
- Alexander Pooth
- Maire Power
- Ben Rakauskas
- Will Waller
- Yan Zhou

[Logos of various funding bodies] and others
OUTLINE

• Company Overview
• Wolfspeed Product Portfolio
• Wafer material selection
• Packaging Choices
  — Metal-Ceramic vs. Plastic
  — Thermal modeling
  — Thermal coefficient of expansion and Die attach selection
  — Plastic overmold selection
  — Qualification and Reliability testing
• High power ceramic product examples
• Plastic packaged product examples
• Summary
UNLOCKING VALUE AND ACCELERATING INVESTMENT AND INNOVATION

CREE \(ightarrow\) Wolfspeed

Power and RF Division

WOLFSPEED IS AN ESTABLISHED, GLOBAL, GROWTH COMPANY

Wolfspeed Facts

- $124M Revenue FY2015
- Double-Digit Growth
- Debt-Free Balance Sheet
- Growth Fueled Organically and Via Acquisition

Headquarters: RTP, NC USA

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GaN PROCESS SUPPORTS MULTIPLE APPLICATION AREAS

- Radar Systems
- EW Jammers
- Telecom
- CATV
- Satcom
- Industrial / Scientific
- Mil Comms
- Tube Replacement

WOLFSPEED RF PRODUCT FAMILY

- Portfolio has about 90 products
- Uses all four released processes
  - G28V3, G50V3, G28V4, G40V4
  - 0.4μm and 0.25μm
**SEMICONDUCTOR WAFFER CHOICES FOR GaN**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Silicon Carbide</th>
<th>Silicon</th>
<th>Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Conductivity</td>
<td>490 W/m-k</td>
<td>150 W/m-k</td>
<td>2200 W/m-k</td>
</tr>
<tr>
<td>Power Density</td>
<td>10 W/mm</td>
<td>0.3X SiC</td>
<td>3X SiC</td>
</tr>
<tr>
<td>Wafers Size</td>
<td>150mm</td>
<td>150mm</td>
<td>150mm</td>
</tr>
<tr>
<td>Cost</td>
<td>Medium</td>
<td>“Low”</td>
<td>High</td>
</tr>
</tbody>
</table>
| Resistivity           | High            | • Doping for high resistivity increases wafer cost  
                              • Decreases with temperature | High |
| Maturity              | >15 years of volume production with 3 suppliers quoting MRL8 | Epitaxy defect density is 10x compared with SiC | Low |
| Adoption              | Wolfspeed, Sunnix, Corvo, Raytheon, Northrup, Integra, UMS, Mitsubishi, Toshiba | MA/Comm, Ohmic | Oorvo, Raytheon (development only) |

**PACKAGING CONSIDERATIONS**

- GaN delivers higher RF power density (~10W/mm) at higher operating temperatures than traditional semiconductors
- Application
  - Radar → High power pulsed
    - Pulse width from 5 to 500 usec
    - Duty cycle from 2 to 20%
  - ISM → Narrow RF bandwidth, high power CW, with high efficiency
  - Jammers / EW → Wide RF bandwidth, CW, with associated low efficiency
  - Telecommunications → Backed-off linear, with high peak to average modulation
- High thermal dissipation requires high conductivity (k) die attach and heat spreader materials
- Coefficient of thermal expansion (CTE) increases with conductivity
- Cost vs. Thermal performance
RF POWER PACKAGE EXAMPLES

CERAMIC AIR CAVITY OR PLASTIC?

<table>
<thead>
<tr>
<th>Air Cavity Ceramic</th>
<th>Plastic Overmold</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Copper Tungsten (CuW) and Copper Molybdenum (CuMo) composite metals provide moderate thermal conductivity with good CTE</td>
<td></td>
</tr>
<tr>
<td>   CTE &lt; 7 ppm/°C</td>
<td></td>
</tr>
<tr>
<td>   k ~ 160 W/m-K</td>
<td></td>
</tr>
<tr>
<td>• Copper /Moly laminates provide a useful trade-off between thermal conductivity &amp; CTE</td>
<td></td>
</tr>
<tr>
<td>   CTE &lt; 10 ppm/°C</td>
<td></td>
</tr>
<tr>
<td>   k &gt; 250 W/m-K</td>
<td></td>
</tr>
<tr>
<td>• Many open tool options</td>
<td></td>
</tr>
<tr>
<td>• Quick design cycle</td>
<td></td>
</tr>
<tr>
<td>• Copper lead frames with high thermal conductivity but high CTE</td>
<td></td>
</tr>
<tr>
<td>   CTE ~ 14 ppm/°C</td>
<td></td>
</tr>
<tr>
<td>   k &gt; 250 W/m-K</td>
<td></td>
</tr>
<tr>
<td>• High tooling costs ~ $400K</td>
<td></td>
</tr>
<tr>
<td>• Not many open toolled options for high power</td>
<td></td>
</tr>
<tr>
<td>• Low cost materials and manufacturing</td>
<td></td>
</tr>
<tr>
<td>• More challenging RF design medium</td>
<td></td>
</tr>
<tr>
<td>• Longer turn-time working with off-shore assembly and test companies (OSAT)</td>
<td></td>
</tr>
</tbody>
</table>

Note – Silicon and Silicon Carbide both have a CTE ~ 4ppm/°C whereas Diamond is about 1ppm/°C
THERMAL MODELING GaN-ON-SiC PRODUCTS

IR MEASUREMENT METHOD

- Fixture and heat spreader surfaces painted black
  - To alleviate concerns with IR emissivity of metallic surfaces
- 1X measurements of package and fixture surfaces
- 15X measurements of die channel
- IR stage temperature = 75°C
- Power dissipation = 167 W
CALIBRATION AND VALIDATION OF THERMAL MODELS

- Thermal model is calibrated by
  - Adjusting the isothermal boundary temperature until the modeled fixture surface matches the IR measurement
  - Adjusting the package to fixture contact resistance until the Flange and Package Base surface temperatures match the IR measurements
- IR measurement of the die surface is averaged over a 5um spot size
  - Expected to be cooler than modeled peak $T_j$ due to IR emissivity
  - Peak $T_j$ can not be measured directly with IR since it is covered by a field plate

<table>
<thead>
<tr>
<th></th>
<th>Measured</th>
<th>Modeled</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixture</td>
<td>90</td>
<td>91</td>
</tr>
<tr>
<td>Flange</td>
<td>103</td>
<td>103</td>
</tr>
<tr>
<td>Package Base</td>
<td>143</td>
<td>143</td>
</tr>
<tr>
<td>$T_j$, average (5um)</td>
<td>187</td>
<td>199</td>
</tr>
<tr>
<td>$T_j$ peak</td>
<td>-</td>
<td>213</td>
</tr>
</tbody>
</table>

THERMAL SIMULATION OF A MULTISTAGE MMIC

- Thermal design is a part of the RF design process
  - Power density and thermal resistance is stage specific
- Thermal simulation needs to include the entire thermal stack
  - CMC heat spreader, 0.25” inch aluminum base plate, and a 0.03 W/mm² interface resistance between package and base, representative of indium foil
VALIDATION OF MATERIALS SYSTEM

- Mismatch between dissimilar materials leads to high mechanical stresses over temperature in the die attach interface
- Thermal cycle testing of die, die attach and heat spreader required
- High power die as used in CGHV31500F have a high aspect ratio
  - Die size $\rightarrow$ ~6mm x 1mm
  - High aspect ratio increases problem

Zero cycles

1000 cycles
PLASTIC PACKAGE SELECTION

• Package outline availability
• Pad size must accommodate the die PLUS offsets required for assembly and reliability
• Design changes may be required to transition from air cavity to plastic due to added parasitics

<table>
<thead>
<tr>
<th>ITEM UNITS</th>
<th>AuSn</th>
<th>Ag Epoxy</th>
<th>Mfr A</th>
<th>Mfr B</th>
<th>Mfr C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk Thermal Conductivity W/m-K</td>
<td>57</td>
<td>23</td>
<td>50</td>
<td>100</td>
<td>180</td>
</tr>
<tr>
<td>CTE ppm/°C</td>
<td>16</td>
<td>38</td>
<td>26</td>
<td>28</td>
<td>22</td>
</tr>
<tr>
<td>Modulus @ RT Gpa</td>
<td>59</td>
<td>3.0</td>
<td>6.7</td>
<td>10</td>
<td>26</td>
</tr>
</tbody>
</table>

DIE ATTACH FOR PLASTIC PACKAGING

• Eutectic solder
  — Inadequate stress relief between SiC and copper LF
  — Limited experience basis at OSATs (off-shore assembly and test)
• Standard Ag epoxy
  — Limited thermal conductivity, k < 30 W/m-K
• Sintered Ag
  ✓ Bulk thermal conductivity, k > 50 W/m-K
  ✓ Modulus on par with Ag epoxy & much lower than AuSn
  ✓ Low sintering temperature minimizes thermal history on LF
  ✓ RoHS / REACh compliant
SINTERED SILVER THERMAL VIABILITY

- Sintered Ag thermally enables high power GaN in plastic
  - $T_{j, \text{peak}} \leq 225^\circ$C realized at $P_{\text{diss}} = 125W$ steady state & $T_{\text{case}} = 105^\circ$C in $175\,\text{mm}^2$ plastic pkg!

  - $T_{\text{shim}} = 80.6^\circ$C
  - $T_{\text{plastic}} = 138.6^\circ$C
  - $T_{j} = 237.7^\circ$C
  - $T_{\text{case}} = 115.7^\circ$C
  - $\Theta_{JC} = 1.27\,\text{C/W}$

  Measured
  - $T_{\text{shim}} = 81^\circ$C
  - $T_{\text{plastic}} = 138^\circ$C

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SINTERED SILVER THERMO-MECHANICAL VIABILITY

- Sintered Ag outperforms AuSn eutectic solder on copper
- 5mm x 1mm GaN-on-SiC die after TC -55 to +125C, 1000 cycles

- .5 milthk AuSn Zero TC

  Nearly 100% delamination!

  Sintered Ag after 1000 TC Negligible degradation!
SINTERED SILVER PROCESS CONSIDERATIONS

- Sintered Ag bondline thickness (BLT)
  - Needs to be small enough to meet thermal requirements
  - And large enough to provide adequate stress relief between die and LF
- Need low voiding for good thermals & fillet for proper stress relief
- Die backside plated Au or Ag to improve adhesion to DA

![Good BLT / Fillet](image1)

![Insufficient BLT with large voids](image2)

C-SAM AND X-SECTION ANALYSIS OF DIE ATTACH

![Diagram of die attach](image3)

![C-SAM and x-section analysis](image4)
**DIE ATTACH PROCESS OPTIMIZATION**

<table>
<thead>
<tr>
<th>Leg</th>
<th>Disperse Pattern</th>
<th>Nozzle Size</th>
<th>Actual Disperse Pattern</th>
<th>Epoxy Coverage (Visual)</th>
<th>Sample Cross section Image</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Single Line</td>
<td>0.2mm</td>
<td><img src="image1" alt="Image" /></td>
<td><img src="image2" alt="Image" /></td>
<td><img src="image3" alt="Image" /></td>
</tr>
<tr>
<td>2</td>
<td>Double Y</td>
<td>0.2mm</td>
<td><img src="image4" alt="Image" /></td>
<td><img src="image5" alt="Image" /></td>
<td><img src="image6" alt="Image" /></td>
</tr>
<tr>
<td>3</td>
<td>Double Y Plus</td>
<td>0.2mm</td>
<td><img src="image7" alt="Image" /></td>
<td><img src="image8" alt="Image" /></td>
<td><img src="image9" alt="Image" /></td>
</tr>
<tr>
<td>Control</td>
<td>Single Line</td>
<td>0.4mm</td>
<td><img src="image10" alt="Image" /></td>
<td><img src="image11" alt="Image" /></td>
<td><img src="image12" alt="Image" /></td>
</tr>
</tbody>
</table>

- All legs met requirements of 100% epoxy coverage and no epoxy voids (as measured by X-ray)
- Leg 1 has excessive voiding in the bond-line
- Leg 2 has best response

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**TEMPERATURE CYCLING**

Zero TC

500 TC

1000 TC
PLASTIC OVERMOLD MATERIALS SELECTION

- Considerations for GaN overmold selection:
  - Thermal suitability for $T_j = 225^\circ$C and weight loss at high temperature
  - Operating temperature range, $T_g$ and resulting CTE stresses with LF, die and die attach fillet
  - Low modulus – compliant enough to handle CTE mismatch to LF
  - Strong adhesion to LF surface, die and die attach fillet
  - Low water absorption for MSL, HAST and THB compliance
  - Mold flow compatibility with selected LF

<table>
<thead>
<tr>
<th>ITEM</th>
<th>UNITS</th>
<th>Mfr A</th>
<th>Mfr B</th>
<th>Mfr C</th>
<th>Mfr D</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_g$</td>
<td>°C</td>
<td>250</td>
<td>190</td>
<td>175</td>
<td>120</td>
</tr>
<tr>
<td>CTE 1</td>
<td>ppm/°C</td>
<td>10</td>
<td>11</td>
<td>7</td>
<td>9</td>
</tr>
<tr>
<td>CTE 2</td>
<td>ppm/°C</td>
<td>60</td>
<td>50</td>
<td>34</td>
<td>40</td>
</tr>
<tr>
<td>Modulus @ RT</td>
<td>Gpa</td>
<td>15.5</td>
<td>15.5</td>
<td>18.5</td>
<td>23.5</td>
</tr>
<tr>
<td>Adhesion (Ag or Au) @ RT</td>
<td>Mpa</td>
<td>10</td>
<td>13.0</td>
<td>14.0</td>
<td>16.0</td>
</tr>
<tr>
<td>Moisture Absorption</td>
<td>%</td>
<td>0.64</td>
<td>0.35</td>
<td>0.22</td>
<td>0.13</td>
</tr>
</tbody>
</table>

PLASTIC OVERMOLD PROCESS CONSIDERATIONS

- Mold temperature / pressure / flow should be tightly controlled to prevent wirebond sway and mold voids
- Post mold cure (PMC) temperature / time important for polymer cross linkaage to yield expected $T_g$, modulus and adhesion

Good processing with no LF delam post-PMC

Improper processing with LF delam post-PMC
PLASTIC OVERMOLD RELIABILITY

- Impact of overmold selection – thermal cycle (TC)
- GaN-on-SiC die post TC -55 to +125C, 1000 cycles

Damage caused by high modulus mold compound

Delamination of passivation layer

Field plate distortion

OVERMOLD PLASTIC PERFORMANCE AT ELEVATED TEMPERATURE

- High temperature operating life (HTOL) and High temperature storage life (HTSL)

Pitting of overmold around gate area post-HTSL

Overmold pitting
QUALIFICATION TESTING

<table>
<thead>
<tr>
<th>Test</th>
<th>Stress</th>
<th>Duration</th>
<th>Devices Sampled</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Temperature Reverse Bias (HTRB)</td>
<td>$125 V_{DS}$, $V_{GS} = -8 V$, $T_s = 125^\circ C$</td>
<td>1000 hrs</td>
<td>75</td>
<td>MIL STD 883G Method 1005</td>
</tr>
<tr>
<td>DC High Temperature Operating Life (HTOL)</td>
<td>$50 V_{DS}$, 96W DC, $T_{j} = 225^\circ C$</td>
<td>1000 hrs</td>
<td>75</td>
<td>MIL STD 883G Method 1005</td>
</tr>
<tr>
<td>Temperature Cycle (TC)</td>
<td>$-55^\circ C$ to $125^\circ C$ 5 min soak</td>
<td>1000 cycles</td>
<td>75</td>
<td>JESD22-A104 Condition B, Soak mode 2</td>
</tr>
<tr>
<td>Humidity (THB)</td>
<td>$85^\circ C$, 85% RH</td>
<td>1000 hrs</td>
<td>75</td>
<td>JESD</td>
</tr>
<tr>
<td>Accelerated Humidity Test (HAST)</td>
<td>$135^\circ C$, 85% RH</td>
<td>96 hrs</td>
<td>75</td>
<td>JESD</td>
</tr>
<tr>
<td>Moisture Sensitivity (MSL)</td>
<td>Level 3, 30°C/60% RH 30 min soak 24°C Reflow</td>
<td>192 hrs Soak</td>
<td>60</td>
<td>MSL3 J-STD-020</td>
</tr>
</tbody>
</table>

HTRB: $V_{DS} = 125 V$, $V_{GS} = -8 V$ FOR 1000 hrs
HTOL: 50V, $P_{Diss} = 96$ W (3 W/mm) FOR 1000 hrs

THB: 85 % RH, 85 °C FOR 1000 hrs
RF LIFE TEST

Pulsed RF 500usec, 10% with 5W/mm Pdiss
Tch = 225°C

Drain Efficiency (%)  
Pout(dBm)

Hours

HIGH POWER CERAMIC PRODUCTS

- Wolfspeed ceramic product portfolio has ~60 devices

CGHV14800
50V, 1000W Peak
L-Band

CGHV31500
50V, 700W Peak
S-Band

CGHV59070
50V, 90W Peak
C-Band

CMPA1D1E025
50V, 40W Peak
Ku-Band
L-BAND 800W PULSED TRANSISTOR – CGHV14800

Features
Input and Output Matched
>15 dB Power Gain
950 W Peak Output Power
65 % Efficiency

S-BAND 500W PULSED 50Ω TRANSISTOR – CGHV31500

Features
Fully Matched for ease of use
>13 dB Power Gain
>650 W Peak Output Power
60% Efficiency
C-BAND PULSED & CW 70W TRANSISTOR – CGHV59070

Features
Input and Output Partial Match
14 dB Power Gain
90 W Peak Power
50 % Efficiency

PLASTIC PACKAGED RF POWER TRANSISTOR PORTFOLIO

- **CGH46006S**
  - 28V, 6W CW
- **CGH27030S**
  - 28V, 30W Peak
  - 4W Average
- **CGHV27015S**
  - 50V, 15W Peak
  - 2W Average
- **CGHV27030S**
  - 50V, 30W Peak
  - 4W Average
- **CGHV1F006S**
  - 40V, 6W Peak
- **CGHV1F025S**
  - 40V, 25W Peak
- **CGHV27660MP**
  - 50V, 60W Peak
  - 10W Average
- **CGHV27030S**
  - 50V, 86W Peak
  - 10W Average
- **CGHV9300MP**
  - 50V, 300W Peak
  - 60W Average
- **CGHV22300MP**
  - 50V, 300W Peak
  - 60W Average
X-BAND 25W TRANSISTOR - CGHV1F025S

Features
- Unmatched for flexibility
- >11 dB Gain
- 25 W Peak Output Power
- 47 % Efficiency

S-BAND 60W PULSED TRANSISTOR - CGHV35060MP

Features
- Pre-matched for high performance
- >14 dB Power Gain
- 75 W Peak Output Power
- 60 % Drain Efficiency
S-BAND 300W TRANSISTOR - CGHV22300MP

Features
18 dB Linear Gain
60 W Average Output Power
32 % Efficiency
-35 dBc Linearity
350 W Peak Power
63 % at Peak Power

WOLFSPEED STATE OF THE ART PACKAGING

<table>
<thead>
<tr>
<th>Package Type</th>
<th>RF Power (W)</th>
<th>RF Power Density (W/cm²)</th>
<th>Power Dissipated (W)</th>
<th>Dissipated Power Density (W/cm²)</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic / CMC CGHV351500</td>
<td>700</td>
<td>250</td>
<td>330</td>
<td>120</td>
<td>S-Band Pulsed Radar 500usec, 10%</td>
</tr>
<tr>
<td>Ceramic / CPC CGHV14800</td>
<td>1000</td>
<td>500</td>
<td>540</td>
<td>270</td>
<td>L-Band Pulsed Radar 5 usec, 5%</td>
</tr>
<tr>
<td>Ceramic / CMC</td>
<td>100</td>
<td>115</td>
<td>110</td>
<td>125</td>
<td>&lt;2 GHz CW</td>
</tr>
<tr>
<td>QFN CGHV1F025</td>
<td>25</td>
<td>210</td>
<td>30</td>
<td>250</td>
<td>X-Band Pulsed Radar 100usec, 10%</td>
</tr>
<tr>
<td>QFN CGHV27030</td>
<td>30</td>
<td>250</td>
<td>10</td>
<td>83</td>
<td>Milcom CW / Linear</td>
</tr>
<tr>
<td>TSSOP CGHV27060</td>
<td>80</td>
<td>280</td>
<td>47</td>
<td>165</td>
<td>&lt;2.7 GHz CW / Linear</td>
</tr>
<tr>
<td>TSSOP CGHV35060</td>
<td>75</td>
<td>260</td>
<td>50</td>
<td>175</td>
<td>S-Band Pulsed Radar 300usec, 20%</td>
</tr>
<tr>
<td>PSOP CGHV22300</td>
<td>350</td>
<td>350</td>
<td>205 (125)</td>
<td>205 (125)</td>
<td>Pulsed 100usec, 10% (Backoff Linear)</td>
</tr>
</tbody>
</table>
SUMMARY

• Industry standard substrate choice for GaN RF power devices is SiC
• Package choice has to be application specific
• Highest single ended power density demonstrated in Air Cavity Ceramic package
• Plastic packaged 300W products with excellent RF performance
• Plastic packaged 25W device at X-band
• Plastic packaging can offer reliable, high performance at lower cost
Cost effective GaN HEMT developments with appropriate thermal transfer

Kazutaka Inoue
Sumitomo Electric Industries, Ltd.

inoue-kazutaka@sei.co.jp

Outline

1. Fundamentals
2. Thermal Study of Substrate
3. Thermal Design (GaN for Radar)
4. Thermal Design (GaN for Base Station)
5. Summary
History of Sumitomo GaN HEMTs

- #1 Volume leader in RF high power GaN
- We strive for
  - Performance
  - Quality
  - Reliability
  - Cost
  - Capacity

Fujitsu, Fujitsu Laboratories
Eudyna Devices
Sumitomo Electric Device Innovations

Development Start → Engineering Sample Release → Mass-production

2013 GaN Market Share
above 5W below 4GHz  Source: ABI Research 2014

WW05 Recent Advances in GaN Power HEMTs Related to Thermal Problems and Low-Cost Approaches
Why GaN?
Johnson's Figure of Merit

**Johnson's FoM**

\[ f_T \times BV = \frac{V_s}{2\pi BF} \]

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>GaAs</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bang Gap Energy (eV)</td>
<td>1.1</td>
<td>1.4</td>
<td>3.2</td>
<td>3.4</td>
</tr>
<tr>
<td>Critical Breakdown Field (MV/cm)</td>
<td>0.3</td>
<td>0.4</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Thermal Conductance (W/cmK)</td>
<td>1.5</td>
<td>0.5</td>
<td>4.9</td>
<td>1.5</td>
</tr>
<tr>
<td>Mobility (cm²/V/s)</td>
<td>1300</td>
<td>6000</td>
<td>600</td>
<td>1500</td>
</tr>
<tr>
<td>Saturated Velocity (*10⁷ cm/s)</td>
<td>1.0</td>
<td>1.3</td>
<td>2.0</td>
<td>2.7</td>
</tr>
</tbody>
</table>

Cost Effective Design, Focused on Thermal Transfer

- Chip cost is determined by ...
  - Wafer process cost and yield
  - Maximum channel temperature design

- Maximum channel temperature is determined by...
  - Reliability of the device technology
  - Thermal conductance of material (on-SiC, on-Si)
  - Chip pattern layout
  - Operating condition
    (Thermal dissipation ↔ Efficiency)
Yield of GaN HEMT Wafer Process

- $\text{Psat} = 52.2 \text{ dBm} \quad \sigma = 0.15$
- $\text{Gp} = 16.6 \text{ dB} \quad \sigma = 0.15$
- $\text{Rth} = 1.2 \text{ °C/W} \quad \sigma = 0.02$

BTS GaN HEMT 2.7GHz 160W, n = 9000 pcs, 181 lots, $\sigma$ = lot average

GaN HEMT wafer process has been refined, through over 10-years mass production.

Reliability of GaN HEMT

- DC-HTOL test ($V_{ds}=60V$, $T_{ch}=250, 275, 300, 315\text{degC}$)
- RF-HTOL test ($V_{ds}=55V$, $T_{ch}=270, 290, 310\text{degC}$, $P_{4\text{dB}}$)

$E_a = 2.10 \text{ eV}$

Material vs. Thermal Design

- Parameters, related to thermal design:
  - Thermal conductance of substrate material (SiC: 4.9, Si: 1.5 [W/cm K])
  - Substrate thickness (Typical thickness is ~100 μm)
  - Gate to gate pitch (Wide pitch improves the degree of heat spreading)

Thermal Design vs. Efficiency

Thermal Dissipation = $P_{dc} - P_{out} + P_{in} = P_{dc} \times (1 - \text{Power-Added-Efficiency})$
Outline

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Case Study of GaN on-Si

RF Performance

GaN HEMT on-Si realize comparable performance to GaN on SiC.

Case Study of GaN on-Si ~ Thermal Design (Sub. Thickness)

1. Simulated Thermal resistance is not comparable, even in 30 μm thickness.

2. Excessive thinning causes chip warping @ GaAs MESFET

Sub. Thickness: 30 μm
Sub. Thickness: 20 μm

Net improvement is limited by chip warping!

Case Study of GaN on-Si ~ Thermal Design (Gate Pitch)

- Thermally equivalent pitch of GaN on-Si is 1.6 times of GaN on-SiC.
- SiC substrate cost used to be several times higher to the wafer process cost. In such cost structure, GaN on-Si was a reasonable solution.
- It should be noted the 1.6 times chip size increases “net wafer process cost” of GaN on Si.
- The power density of GaN HEMT has been increasing. It used to be ~5 W/mm, but now reaches to ~10 W/mm. Higher power density favors better thermal conductance material.
Case Study of GaN on-Si
～Thermal Design (Chip Stretch)

Two options to realize thermally equivalent GaN on-Si

<table>
<thead>
<tr>
<th></th>
<th>Option.1 (Lateral Stretch)</th>
<th>Option.2 (Vertical Stretch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>on-SIC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>on-Si</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Effect</td>
<td>- Larger PKG is required for on-Si chip.</td>
<td>- Larger unit finger increases gate resistance, which degrades the gain by more than 1dB.</td>
</tr>
<tr>
<td>PKG for on-SiC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PKG for on-Si</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Judgement</td>
<td>Total cost strongly depends on PKG price.</td>
<td>Trade-off issue arises (vs. gain).</td>
</tr>
</tbody>
</table>

GaN on-SiC is the best solution at present, judging from both cost and RF property.

In addition...
～SiC Quality Improvement

- SiC quality was one of the issues to be solved.
- The current SiC has realized smooth surface, and it contributes to the drastic improvement of the GaN on SiC cost structure.
Prospect of Substrate Material

- Power density of GaN HEMT have been increased, and will be continued.
- The benchmark of GaN on Si vs. SiC indicates the availability of GaN on diamond.

<table>
<thead>
<tr>
<th></th>
<th>2005</th>
<th>2016</th>
<th>2025</th>
</tr>
</thead>
<tbody>
<tr>
<td>on-Si</td>
<td>RF-loss elimination required</td>
<td>Thermal limitation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>No more cost effective</td>
<td></td>
<td>--</td>
</tr>
<tr>
<td>on-SiC</td>
<td>Expensive &amp; many defects</td>
<td>Most promising</td>
<td>Will be most promising</td>
</tr>
<tr>
<td></td>
<td>Chip selection needed</td>
<td></td>
<td>Thermal design may be critical @ &gt;20W/mm</td>
</tr>
<tr>
<td>on-diamond</td>
<td>--</td>
<td>Similar to early stage SiC ?</td>
<td>Competitive @&gt;20W/mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Quality &amp; cost required</td>
</tr>
</tbody>
</table>

Higher power density favors better thermal conductance material.

Outline

1. Fundamentals
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4. Thermal Design (GaN for Base Station)
5. Summary
Slide 19

Output Power vs. Frequency

- **Satellite**
  - CW operation
- **Case.2 BTS**
  - Backed-off operation
- **Case.1 Radar**
  - Pulsed operation

---

Slide 20

**Satellite Application**

(CW-operation, as a reference)

Over 74% Efficiency, L-Band 200W GaN-HEMT for Space Applications


- Designed for CW and saturated operation. (Most severe thermal requirement)
Case.1 Rader (Pulsed operation)

- Thermal design of pulsed operation chip differs from CW one, and the estimation of the transitional Tch is important. The following slides explain the detail.

Channel Temperature Simulation using Transient Thermal Resistance

- During the pulse-ON, channel temperature rises due to the heat generation.
- At the pulse-OFF, the channel temperature falls down by heat dissipation, which is expressed as reverse behavior of heat generation.
- With combining these 2 lines, the channel temperature falls.
Channel Temperature Simulation using Transient Thermal Resistance

- The peak $T_{ch}$ at the 1st pulse is calculated as shown in above.
- The 2nd peak $T_{ch}$ is also calculated, combining these 3 values.
- The total $T_{ch}$ rise is summation of the delta $T_{ch}$ at each on-state condition.

$$dT_{ch} \text{ peak 1} = P_d \cdot R_{th} (\tau)$$

$$dT_{ch} \text{ peak 2} = P_d \cdot \{R_{th}(T+\tau)-R_{th}(T)+R_{th}(\tau)\}$$

$$dT_{ch} \text{ peak 3} = P_d \cdot \{R_{th}(2T+\tau)-R_{th}(2T)+R_{th}(T+\tau)-R_{th}(T)+R_{th}(\tau)\}$$

Channel Temperature Measurement & Analysis

- The analysis performed more than 10 years ago. We only had an IR system with rather slow shutter speed. But we found the measured $T_{ch}$ from IR agreed with the simulated $T_{ch}$ curve, by taking the shutter speed into consideration.
- Thus, we concluded that the mentioned simulation in previous slide is reliable. And the compact kW-class GaN device was developed by utilizing this analysis.
kW-Class GaN HEMT Pallet Amplifier for Radar

Size: 58.5 mm X 40.0 mm X 8.0 mm
- Input/Output matched to 50 ohm
- Includes RC Bias Circuit
- Cu base


kW-Class GaN for Radar RF Performance

- $V_{DD}=65$ V, $f=2.9$ GHz
  - Output Power: 59.4 dBm
  - Drain Efficiency: 55.0%
  - Gain: 13.8 dB

- $V_{DD}=80$ V, $f=3.2$ GHz
  - Output Power: 60.0 dBm
  - Drain Efficiency: 49.5%
  - Gain: 14.1 dB

➢ Compact 1 kW class GaN HEMT for radar application has successfully demonstrated, by optimizing for pulsed operation.
Prospect of Cost Effective GaN for Radar applications

- Using GaN to replace the klystron
  - High reliability, Maintenance free
  - Compact, Easy operation
  - Reduction of OPEX

- GaN output power is not as large as klystron, but it allows long pulses. Pulse compression can be used.

- Cost effective GaN HEMT will penetrate into the radar applications.

Outline

1. Fundamentals
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Case. 2 BTS Application (Backed-off Operation)

BTS trend → Smaller → Higher efficiency

**Both efficiency improvements of device itself & efficiency enhancement circuit techniques are required, at backed-off power region.**

Operation Class (F, inverse-F)
Combination of Inv. Class-F & GaN HEMT Property

- Inverse Class-F requirements are,
  - Low Ron (Steep Knee) reduces RF-loss
  - High breakdown voltage contributes to keep good pinch off
- GaN HEMT is the best technology for these requirements at present.

Circuit of Inverse Class-F 100W GaN HEMT

**Design Concept**
- Circuit: Harmonic tune by simple (=low cost) LC circuit (LPF)
- GaN chip: Size minimization by referring thermal loss
Theory of Doherty Amplifier

(a) Backed-off

Class-B or AB

Class-C

Main Amp.

Zopt

2xZopt

Peak Amp. OFF

Zopt/2

λ/4

Peak Power

(b) Peak Power

Class-C

Main Amp.

Zopt

λ/4

Zopt/2

Peak Amp. ON

Zopt

λ/4

Peak Amp. OFF

Open

Power Matching

Zopt

Efficiency Matching

Zopt

2xZopt

 depend on
main amp's eff.

depend on both main and peak amp's eff.

WW05 Recent Advances in GaN Power HEMTs Related to Thermal Problems and Low-Cost Approaches

GaN HEMT for Doherty PA

c) Cds Key of High Frequency Performance

70W-class Device for 2.6GHz Base Stations

<table>
<thead>
<tr>
<th>70W-class Device</th>
<th>Vds</th>
<th>Imax</th>
<th>Wg</th>
<th>Cds</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si LDMOS-FET</td>
<td>28V</td>
<td>26A</td>
<td>120mm</td>
<td>31pF</td>
</tr>
<tr>
<td>GaN HEMT (This work)</td>
<td>50V</td>
<td>11A</td>
<td>18mm</td>
<td>3.8pF</td>
</tr>
</tbody>
</table>

RF Performance of Doherty PA

Input Power [dBm] vs. Output Power [dBm], Gain [dB]

Vds = 50V, Idq-m = 200mA Idq-p : Class-C Bias
f = 2.6GHz, CW Pulse Duty = 10% (6μs/60μs)

Conventional Device vs. C_{ds}-reduced Device

Freq.=2.57GHz, Vds=50V


Example of Envelope Tracking (ET)

Conventional Operation vs. Envelope Tracking Operation


GaN HEMT for Envelope-Tracking
1. Cds reduction & Vds dependence reduction
2. BV_{dsx} ≥ 300 V, for 20-65V ET-operation

Imax = 680mA/mm, Cds=0.15pF/mm, BV_{dsx} ≥ 300V

Optimum Thermal Design for BTS

1. Thermal Design

![Graph showing thermal design dependence on efficiency]

2. Efficiency Boosting

<table>
<thead>
<tr>
<th>Circuit Technique</th>
<th>~2005</th>
<th>2006</th>
<th>2009</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Eff. @8dB-B.O.</td>
<td>34%</td>
<td>45%</td>
<td>55%</td>
<td>68%</td>
</tr>
<tr>
<td>Thermal Dissipation</td>
<td>Ref.</td>
<td>83%</td>
<td>68%</td>
<td>48%</td>
</tr>
</tbody>
</table>

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RRH* BTS-system and GaN HEMT

* Remote Radio Head

CAPEX (Capital Expenditure) -> Cost reduction of GaN itself has been progressed, and small & light weight PA, utilizing GaN high efficiency, contributes to BTS setting cost.

OPEX (Operating Expenditure) -> Higher efficiency PA realizes lower power consumption.

WW05 Recent Advances in GaN Power HEMTs Related to Thermal Problems and Low-Cost Approaches
Outline

1. Fundamentals
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4. Thermal Design (GaN for Base Station)
5. Summary
GaN HEMTs have already realized high quality, uniformity and reliability for infrastructure RF power applications. Thus, the cost reduction has been strongly required.

The adequate thermal transfer design is one of the solutions. GaN on-SiC has been proved the best material to satisfy both the cost and thermal requirements. The focus design on pulsed operation is effective for compact radar devices, and the efficiency boosting in backed-off region have reduced the chip size of base station PAs.

Quality
- SiC crystal, Epi-growth uniformity, Small process deviation

Reliability
- Stringent qualification, Ruggedness

Cost
- Adequate thermal design, utilizing SiC material property

GaN HEMT to various applications (Satellite, Radar, Base station)

Summary (2/2)

GaN HEMT has already been adopted in several markets. For further market penetration, continuous cost down efforts are essential.
Cost effective approaches for European GaAs & GaN Power solutions

Guillaume CALLET

guillaume.callet@ums-gaas.com

Outlining

What can be the reducing cost drivers for GaN on SiC solution?

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
- Conclusions
Outline

- Presentation of UMS
  - III-V company with 20 year experience in semiconductor (especially GaAs HEMT)
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
- Conclusions

UMS at a glance

- Founded in 1996 by gathering Thales and AIRBUS Defense and Space GmbH activities
- European source of RF MMIC solutions, GaAs and GaN foundry services
- 2 industrial facilities in Ulm (Germany) & Villebon (France)
- 400 people
Outilne

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
- Conclusions

UMS GaN technologies

<table>
<thead>
<tr>
<th>Status</th>
<th>GH50</th>
<th>GH25</th>
<th>GH15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Released</td>
<td>Released</td>
<td>To be</td>
<td></td>
</tr>
<tr>
<td>Design kit available</td>
<td>Design kit available</td>
<td>released 2017</td>
<td></td>
</tr>
<tr>
<td>Targeted Performances</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate length</td>
<td>0.50µm</td>
<td>0.25µm</td>
<td>0.15µm</td>
</tr>
<tr>
<td>Power</td>
<td>5 W/mm</td>
<td>4 W/mm</td>
<td>3.5 W/mm</td>
</tr>
<tr>
<td>Operating Vds</td>
<td>50 V</td>
<td>30 V</td>
<td>20V</td>
</tr>
<tr>
<td>Breakdown voltage (Vbds)</td>
<td>&gt;200 V</td>
<td>&gt;120 V</td>
<td></td>
</tr>
<tr>
<td>MTF</td>
<td>1e6 / 200°C</td>
<td>1e6 / 200°C</td>
<td>1e6 / 200°C</td>
</tr>
<tr>
<td>Domain of frequencies</td>
<td>Up to 7 GHz</td>
<td>Up to 20 GHz</td>
<td>Up to 40GHz</td>
</tr>
</tbody>
</table>

Power by die (W)

Frequency (GHz)

New Development

GH50 Power bar

GH25 MMIC
Outline

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
  - Various Packaging solutions
  - Thermal management of QFN
    - PCB / Glue / Die Coating
- UMS Products & Foundry Solutions
- Conclusions

Packaging offer for power

Main constraints for GaN packaging - related to costs:
- Frequency band
- Thermal management
Thermal management analysis

Different solutions investigated:

- Package solutions:
  - Flange
  - Ceramic metal SMD
  - SMD QFN
- Stack variation
  - PCB variations
  - Interlayer stack
    - Mo / Diamond Tab
    - CuMo Coin

- SMD QFN package is excellent
- Flange packages are competitive up to 20GHz
  - Package optimization still ongoing to achieve VSWR <1.5:1 at 20GHz
  - Part of the matching can be integrated into the die
Package Thermal analysis

Target: Package GH50 & GH25 products

- Analysis must be carried out on different samples:
  - Power-bares
  - MMICs
- Finite element simulations performed on different 3 mains package family – ANSYS

MMIC Packaging: Modeling assumption

Analysis performed on ANSYS:

- Symmetry: ¼ of the device is meshed
- GaN/SiC interface → Layer with low thermal conductivity (TBR)
- Joule heating → Block heater along drain edge of gate foot (≈ 1.5 µm)
- Boundary condition → Fixed temperature on backside of full assembly
- Meshing → Specific methodology for power bars ≈ 1 000 000 nodes

2nd stage
P_{diss}@14GHz & 34dBm ≈ 3.8 W/transistor
8 transistors → 30.4W
P_{diss} = 3.16W/mm

1st stage
P_{diss}@14GHz & 34dBm ≈ 2 W/transistor
8 transistors → 16W
P_{diss} = 2W/mm

Test Vehicle GH25 MMIC:
1st stage: 4x8x125µm
2nd stage: 8x8x150µm
## Flange Package

\[ T_c = 80^\circ C / P_{diss} : 2nd \text{ stage} \rightarrow 3.16 \text{ W/mm (30.4 W)} / 1st \text{ stage} \rightarrow 2 \text{ W/mm (16 W)} \]

<table>
<thead>
<tr>
<th>Cases</th>
<th>Flange KYO</th>
<th>Flange KYO + Tab Mo</th>
<th>Flange + Tab Diamond</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stack</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{th _tot} ) (°C/W)</td>
<td>3.75</td>
<td>3.84</td>
<td>3.24</td>
</tr>
<tr>
<td>( T_{j _max} ) (°C)</td>
<td>194</td>
<td>196.8</td>
<td>178</td>
</tr>
</tbody>
</table>

## Ceramic metal SMD

\[ T_c = 80^\circ C / P_{diss} : 2nd \text{ stage} \rightarrow 3.16 \text{ W/mm (30.4 W)} / 1st \text{ stage} \rightarrow 2 \text{ W/mm (16 W)} \]

<table>
<thead>
<tr>
<th>Cases</th>
<th>SMD &amp; PCB coin</th>
<th>SMD &amp; PCB vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stack</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{th _tot} ) (°C/W)</td>
<td>5.06</td>
<td>4.69</td>
</tr>
<tr>
<td>( T_{j _max} ) (°C)</td>
<td>233.8</td>
<td>222.7</td>
</tr>
</tbody>
</table>
Plastic Package SMD QFN

Rtc = 80°C / Pdiss : 2nd stage ➔ 3.16 W/mm (30.4 W) / 1st stage ➔ 2 W/mm (16 W)

### Cases

<table>
<thead>
<tr>
<th>Cases</th>
<th>SMD &amp; PCB coin</th>
<th>SMD &amp; PCB vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stack</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rth_tot (°C/W)</td>
<td>4.97&lt;sup&gt;a&lt;/sup&gt;</td>
<td>4.72&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
<tr>
<td>Tj_max (°C)</td>
<td>231&lt;sup&gt;a&lt;/sup&gt;</td>
<td>224&lt;sup&gt;b&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

2 different Ag based glues evaluated:
- a) 20 W.m<sup>-1</sup>.K<sup>-1</sup>
- b) 70 W.m<sup>-1</sup>.K<sup>-1</sup>

### Synthesis

<table>
<thead>
<tr>
<th>Case study</th>
<th>Packaging</th>
<th>Remark</th>
<th>Rth (°C/W)</th>
<th>Bandwidth</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Flange KYO</td>
<td>Hermetic</td>
<td>3.75</td>
<td>Up to 6 GHz</td>
<td>☀</td>
</tr>
<tr>
<td>2</td>
<td>Flange KYO + Mo TAB</td>
<td>Hermetic</td>
<td>3.84</td>
<td>Up to 6 GHz</td>
<td>☀</td>
</tr>
<tr>
<td>3</td>
<td>Flange KYO + Diamond TAB</td>
<td>Hermetic</td>
<td>3.25</td>
<td>Up to 6 GHz</td>
<td>☀</td>
</tr>
<tr>
<td>4</td>
<td>SMD + PCB coin</td>
<td>Hermetic</td>
<td>5.06</td>
<td>Up to 14 GHz</td>
<td>☀</td>
</tr>
<tr>
<td>5</td>
<td>SMD + PCB via</td>
<td>Hermetic</td>
<td>4.69</td>
<td>Up to 14 GHz</td>
<td>☀</td>
</tr>
<tr>
<td>6</td>
<td>SMD QFN + PCB coin</td>
<td>Die attach : 20 W.m&lt;sup&gt;-1&lt;/sup&gt;.K&lt;sup&gt;-1&lt;/sup&gt;</td>
<td>4.97</td>
<td>&gt; 20 GHz</td>
<td>☀</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Die attach : 70 W.m&lt;sup&gt;-1&lt;/sup&gt;.K&lt;sup&gt;-1&lt;/sup&gt;</td>
<td>4.72</td>
<td>&gt; 20 GHz</td>
<td>☀</td>
</tr>
<tr>
<td>7</td>
<td>SMD QFN + PCB via</td>
<td>Die attach : 20 W.m&lt;sup&gt;-1&lt;/sup&gt;.K&lt;sup&gt;-1&lt;/sup&gt;</td>
<td>4.56</td>
<td>&gt; 20 GHz</td>
<td>☀</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Die attach : 70 W.m&lt;sup&gt;-1&lt;/sup&gt;.K&lt;sup&gt;-1&lt;/sup&gt;</td>
<td>4.32</td>
<td>&gt; 20 GHz</td>
<td>☀</td>
</tr>
</tbody>
</table>
Approach power bar assembly

Temperature Gradient

- $8\times8\times400\mu m$ / $T_{ref} = 75^\circ C$ / $P = 2W/mm$ / CW

$T_{j\_Peak} = 211.9^\circ C$

<table>
<thead>
<tr>
<th>Material</th>
<th>$T(\degree C)$</th>
<th>$\Delta T (\degree C)$</th>
<th>$R_{th}(\degree C/W)$</th>
<th>Contribution (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN / TBR</td>
<td>217.9</td>
<td>21.4</td>
<td>0.418</td>
<td>15.0</td>
</tr>
<tr>
<td>substrat SiC</td>
<td>196.5</td>
<td>18.2</td>
<td>0.355</td>
<td>12.7</td>
</tr>
<tr>
<td>colle puce ($40W/mK$)</td>
<td>178.3</td>
<td>15.6</td>
<td>0.304</td>
<td>10.9</td>
</tr>
<tr>
<td>Leadframe</td>
<td>162.7</td>
<td>12.7</td>
<td>0.248</td>
<td>8.9</td>
</tr>
<tr>
<td>BrasureSnPb</td>
<td>150.0</td>
<td>23.7</td>
<td>0.463</td>
<td>16.6</td>
</tr>
<tr>
<td>CI/glue</td>
<td>126.3</td>
<td>30.3</td>
<td>0.591</td>
<td>21.2</td>
</tr>
<tr>
<td>Drain Al</td>
<td>96.1</td>
<td>21.1</td>
<td>0.411</td>
<td>14.7</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>75</strong></td>
<td><strong>142.9</strong></td>
<td><strong>2.792</strong></td>
<td><strong>100.0</strong></td>
</tr>
</tbody>
</table>

Die Attach Impact

- $8\times8\times400 / 7x7$ QFN, CW, $P=2W/mm$, $T_{case}=75^\circ C$, Cond glue = 40W/m.K

<table>
<thead>
<tr>
<th>Material</th>
<th>$T(\degree C)$</th>
<th>$\Delta T (\degree C)$</th>
<th>$R_{th}(\degree C/W)$</th>
<th>Contribution (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN / TBR</td>
<td>230.9</td>
<td>22.0</td>
<td>0.430</td>
<td>14.1</td>
</tr>
<tr>
<td>substrat SiC</td>
<td>208.9</td>
<td>18.4</td>
<td>0.360</td>
<td>11.8</td>
</tr>
<tr>
<td>colle puce ($40W/mK$)</td>
<td>190.5</td>
<td>28.9</td>
<td>0.565</td>
<td>18.6</td>
</tr>
<tr>
<td>Leadframe</td>
<td>161.6</td>
<td>12.1</td>
<td>0.235</td>
<td>7.7</td>
</tr>
<tr>
<td>BrasureSnPb</td>
<td>149.5</td>
<td>23.3</td>
<td>0.455</td>
<td>14.9</td>
</tr>
<tr>
<td>CI/glue</td>
<td>126.2</td>
<td>30.1</td>
<td>0.588</td>
<td>19.3</td>
</tr>
<tr>
<td>Drain Al</td>
<td>96.1</td>
<td>21.1</td>
<td>0.411</td>
<td>13.5</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>75</strong></td>
<td><strong>155.9</strong></td>
<td><strong>3.046</strong></td>
<td><strong>100.0</strong></td>
</tr>
</tbody>
</table>
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GH50 Power Bar / Transient

- 8x8x400 / 7x7 QFN / Tref = 75°C / P = 2W/mm

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Conclusion on assembly

- SMD QFN solutions are broadband and lower cost solution
  ➔ Applied to GH25 and GH50
- Analysis shows that thermal management strongly depends on the PCB
  - Coin offers very good thermal dissipation / difficult to implement to series
  - Thermal glue can reduce by roughly 0.2 W.m⁻¹.K⁻¹
- As demonstrated GaN on SiC packaged in QFN can also operate in CW
  - Important care must be take to the functioning conditions
Outiline

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution

UMS Products & Foundry Solutions
  - Foundry Presentation
    - Market addressed are not only military
    - Foundry partner contribution
  - Quasi-MMIC solution development
    - Concept: Combination of GaN & GaAs
    - Cost reduce
    - Solutions

Conclusions

UMS Foundry Solutions
1W High Power Amplifier 37-40GHz

PPH15X-20

Power detector inside, Gain Control

Advanced concept / PPH15X-20 / QFN / CHA6194-QXG

- **Application**
  - Point to point
  - Point to Multipoint

- **Specific features:**
  - GaAs pHEMT process
  - Power detector dynamic 30dB
  - Low AM/AM, AMP/PM,
  - QFN 5x6

- **High linearity HPA**
  - RF bandwidth: 37-40GHz
  - Linear Gain: 20dB
  - Power at 1dB comp.: 30dBm
  - Sat. Power: 31dBm
  - RL>13dB
  - Consumption: 6V, 0.8A

Vd=6V Idq=0.8A

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Vd=6V Idq=0.8A

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Foundry Portfolio

QFN Assembly offer for all processes

GH50 & GH25 Foundry key figures

- GH25: Since 2010 more than 130 wafers processed in the frame of 80 different projects
- GH50: Production launched and transferred to 4”
- More 150 wafers to be manufactured in both GH50 & GH25 in 2016
- Design Kit including EM Stack and DRC for ADS2016
DK available for GH25-10

**GH25: MMIC process: Qualified & Open in Foundry**
- 250nm gate length
- On 4-inch SiC wafer
- Frequency range: DC – 20 GHz
- $V_{ds} = 30V$ as standard Recommended Operating Value
- $I_{dss} = 850 mA/mm$ as average value
- Very High breakdown voltage: $V_{bds} > 120V$
- Power density: 4W/mm @ 10GHz in CW Mode
- Design Kit available for ADS2009-2016 & MWO
  - NL model for Hot FET (electrothermal)
  - L FET model for noise
  - NL model for Cold-FET
  - NL model for diodes
  
(Scalable models for passives and active elements)
- New features: DRC & Stack EM available for ADS2016

---

**ANSYS/ADS Thermal analysis**

- Transistor GH25 8x125 d’UMS / $V_{ds}=25V$ $I_{ds}=25mA/mm$

![](image-url)
TNO – HPA GH25-10 design

**THERMAL SIMULATION**

- Input stage 1x10x275um, $P_{diss}=8.2$ W
- Output stage 4x10x275, $P_{diss}=23.3$ W
- Matching networks, $P_{diss}=7.2$ W

\[ = P_{diss\_total} - (\text{input+output stage}) \]

**MATERIAL PARAMETERS**

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal conductivity ($W/mK$)</th>
<th>Heat Capacity ($J/kgK$)</th>
<th>Density ($kg/m^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5C (cold case)</td>
<td>330</td>
<td>1.5</td>
<td>600</td>
</tr>
<tr>
<td>Gold</td>
<td>317</td>
<td>12</td>
<td>18000</td>
</tr>
<tr>
<td>MAMIC 2P1A1A</td>
<td>20</td>
<td>235 ($t_{33}$)</td>
<td>4000 ($t_{50}$)</td>
</tr>
<tr>
<td>Copper QFN</td>
<td>380</td>
<td>388</td>
<td>8700</td>
</tr>
</tbody>
</table>

**In courtesy of TNO**

**UMS product Solutions**
** CHK015A-QBA **

** DC - 6 GHz Packaged Transistor **

- ** Specific feature **
  - Wide-band
  - Low parasitic Plastic Package
  - Low thermal resistance

- ** Application **
  - *Radar & Communications*

<table>
<thead>
<tr>
<th>General Purpose Transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF bandwidth: DC – 6GHz</td>
</tr>
<tr>
<td>Linear Gain: 14dB @ 6GHz</td>
</tr>
<tr>
<td>Output Power: &gt; 15W</td>
</tr>
<tr>
<td>Drain Efficiency: &gt; 70%</td>
</tr>
<tr>
<td>PAE: 50% @ 6GHz</td>
</tr>
<tr>
<td>Package: DFN 3x4</td>
</tr>
</tbody>
</table>

---

** 25W / X-band / QFN **

- ** Application **
  - *Defence / Space*

<table>
<thead>
<tr>
<th>Main Performances</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF bandwidth: 8.5 – 10.5GHz</td>
</tr>
<tr>
<td>Gain: 30dB</td>
</tr>
<tr>
<td>Pout : 25W</td>
</tr>
<tr>
<td>PAE-associated: 45%</td>
</tr>
<tr>
<td>Consumption: 30V, 0.8A</td>
</tr>
</tbody>
</table>

---

- ** Specific feature **
  - High efficiency
  - High power
  - Die / 15W version available in QFN
Quasi MMIC Concept

Use of UMS proprietary Passive MMIC Technology: Q-MMIC is close to MMIC size

Input Matched Circuit + GaN Power Bar + Output Matched Circuit

Fast design & fabrication ☺ ☺ ☺

50Ω 50Ω

Customize your Q-MMIC

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Why “Quasi MMIC”? 

- **Integration**
  - Close to MMIC size

- **Cost**
  - Close to hybrid solutions

- **Flexibility**
  - Short dev. cycle times (passive MMICs)
    - GH50/25: 14 Weeks ICT
    - URLC: 5 Weeks

Example of 50W C-band HPA

Applicable to QFN for low cost development

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**100W / L-band / QFN**

*In development / GH50 based / Internally-Matched / Q-MMIC*

- **Specific feature @ 1.3GHz**
  - Peak Pout=110W
  - With PAE=57%
  - Gain = 14dB

- **Application**
  - Radar / Dual Use

- **Main Performances**
  - RF bandwidth: 1.2 – 1.4GHz
  - Linear Gain: 15dB
  - Output Power: 100W
  - Gain @ 50W: 10dB
  - PAE: 57%
  - Package: DFN 7x7

---

**50W / C-band / QFN**

*In development / GH25 based / Internally-Matched / Q-MMIC*

- **Specific feature**
  - High PAE
  - Low parasitic Power Plastic Package
  - Low thermal resistance

- **Application**
  - Radar & Communications

- **Main Performances**
  - RF bandwidth: 5.2 – 5.9GHz
  - Linear Gain: 14dB
  - Output Power: 50W
  - Gain @ 50W: 10dB
  - PAE: 45%
  - Package: DFN 7x7

---

"High Performance Plastic Packaged 100W L-Band Quasi-MMIC HPA" D. Bouw et al. - EuMC06-05
C-band DPA Description

Symmetric DPA Architecture / GH25 based / Q-MMIC / QFN packaging

- Application
  - Communications / 5G

Main Objectives
- Configuration
  - 1 stage => for investigations purpose
    - Single & dual input
    - Linearity / Main & Peak synchronization...
- Key Performance
  - Frequency band: 5.6 – 6.6GHz
  - Peak Output Power: 15W
  - PAE @ 6dB OBO: > 35%

C-band DPA Characterizations

PAE vs Freq / 6 & 10dB OBO / 4 Boards / T=25°C

- Biasing conditions:
  - Vd = 30V
  - Id_q_main = 60mA / Vgs0_peak = -7V

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Slide 38
Outline

- Presentation of UMS
- Overview of GaN technologies
- Thermal analysis for the development of packaged GaN solution
- UMS Products & Foundry Solutions
- Conclusions

Conclusions

- QFN Solution validated for power technologies up to 40GHz – including GaN
  - MMIC in QFN for GH25 validated with enhanced glue + PCB solutions
    - High efficiency solutions already available
  - Q-MMIC in QFN used for GH50 & GH25
    - Challenging solutions evaluated
  - Release of PPH15X-20 for applications up to 40GHz

- Foundry access allowing more and more QFN assembly
  - Tools available for ADS allow more accurate thermal analysis
  - Association with URC (passive process) available in Foundry
  - Indicators allow to identify the cost decrease (Industrial Manufacturing cycle time reducing, ...)

- Final passivation is under development and should be available to improve the robustness versus humidity for GH50/GH25/URLC
• TNO for their participation
• Colleagues for their support & works
  – M. Camiade
  – P-F. Alleaume
  – L. Brunel
  – M. Feron
  – E. Leclerc
  – J-P. Viaud